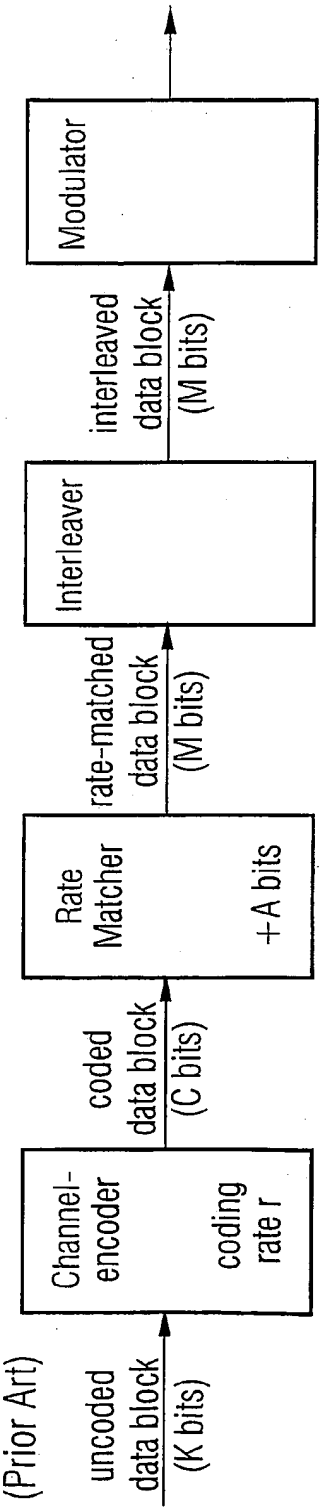


FIG.1a
(Prior Art)

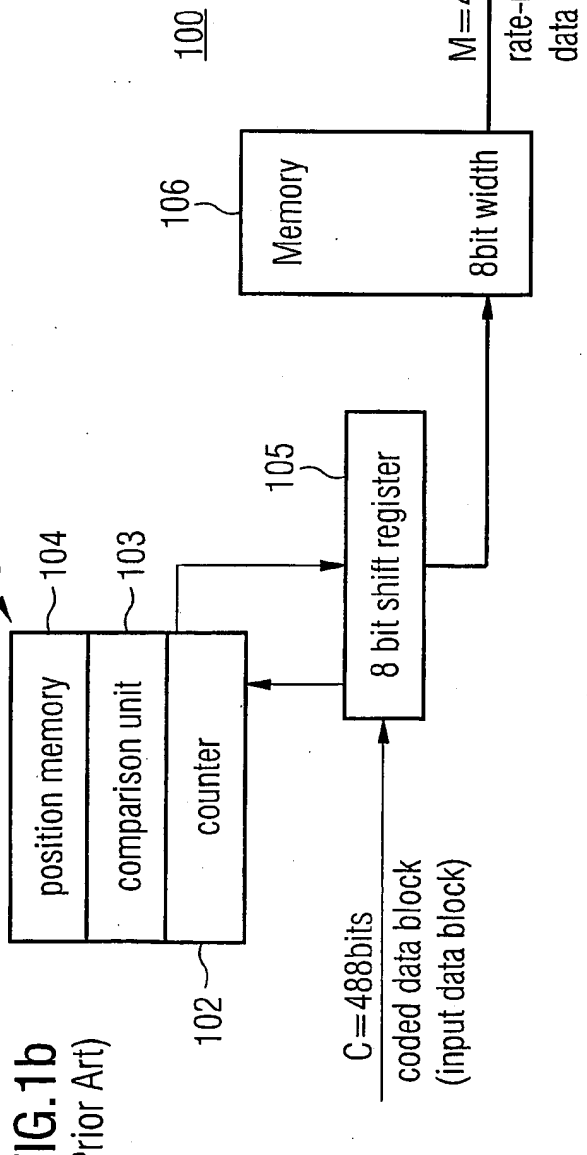


FIG.1b
(Prior Art)

FIG. 2

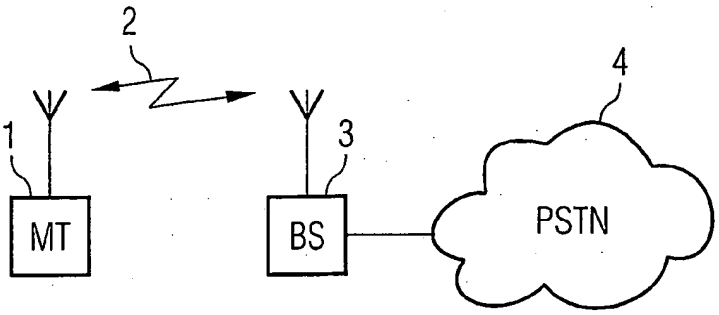


FIG. 3

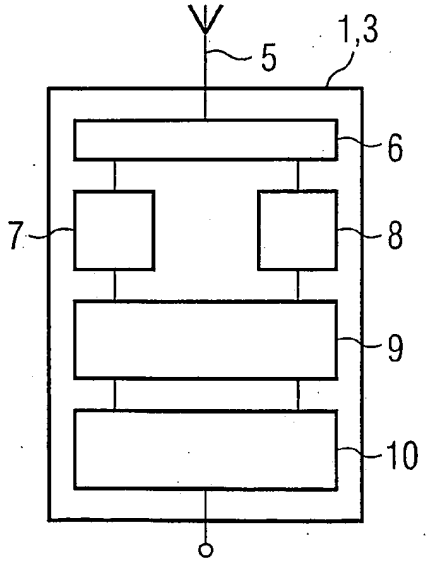


FIG. 4

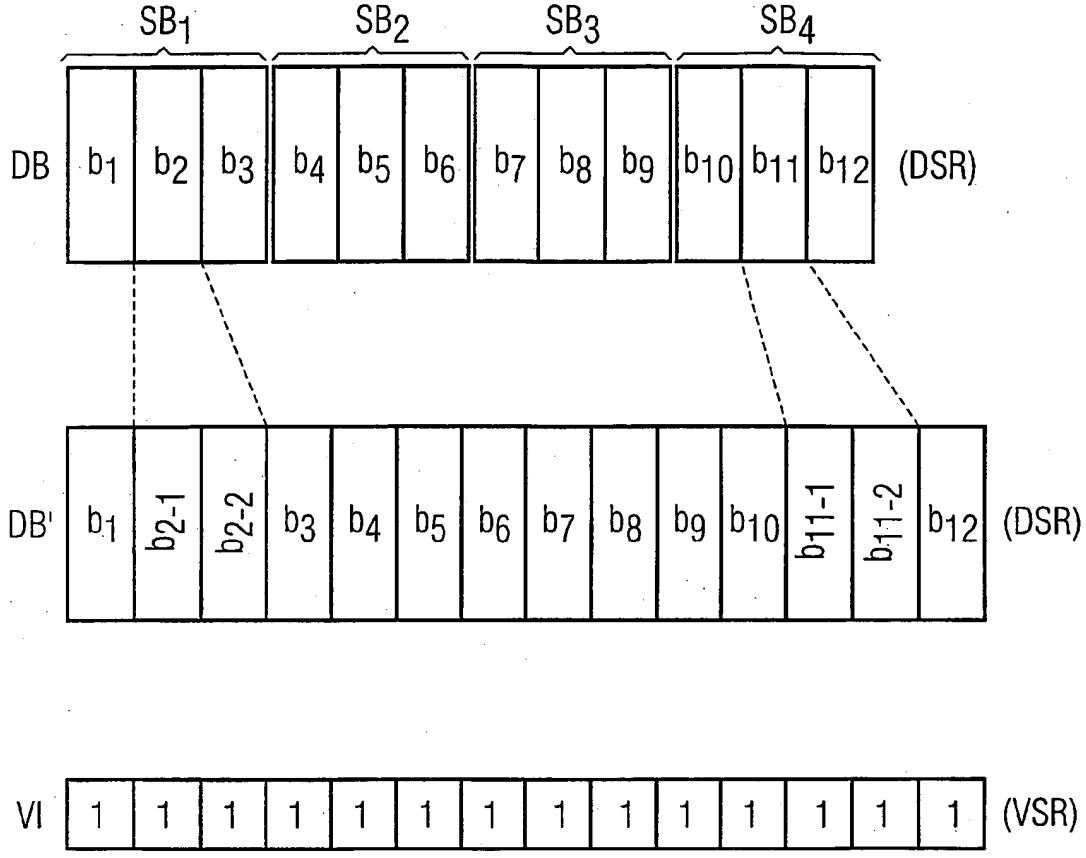

SB1
SB2
SB3
SB4
DB
b1 b2 b3 b4 b5 b6 b7 b8 b9 b10 b11 b12
(DSR)
DB'
b1 b2-1 b2-2 b3 b4 b5 b6 b7 b8 b9 b10 b11-1 b11-2 b12
(DSR)
VI
1 1 1 1 1 1 1 1 1 1 1 1 1 1
(VSR)

FIG. 5

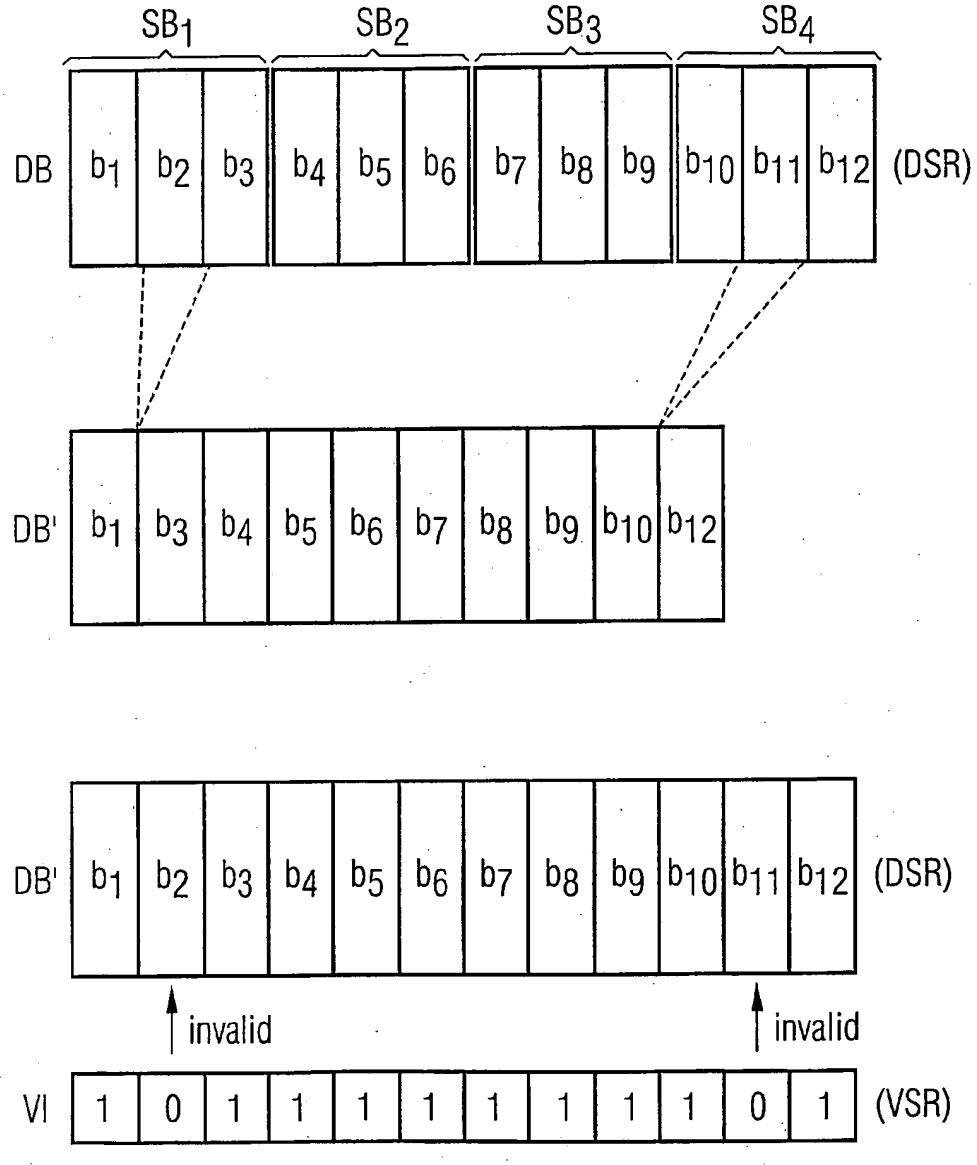

SB1
SB2
SB3
SB4
DB
b1 b2 b3 b4 b5 b6 b7 b8 b9 b10 b11 b12
(DSR)
DB'
b1 b3 b4 b5 b6 b7 b8 b9 b10 b12
DB'
b1 b2 b3 b4 b5 b6 b7 b8 b9 b10 b11 b12
(DSR)
invalid
invalid
VI
1 0 1 1 1 1 1 1 1 1 0 1
(VSR)

FIG. 6

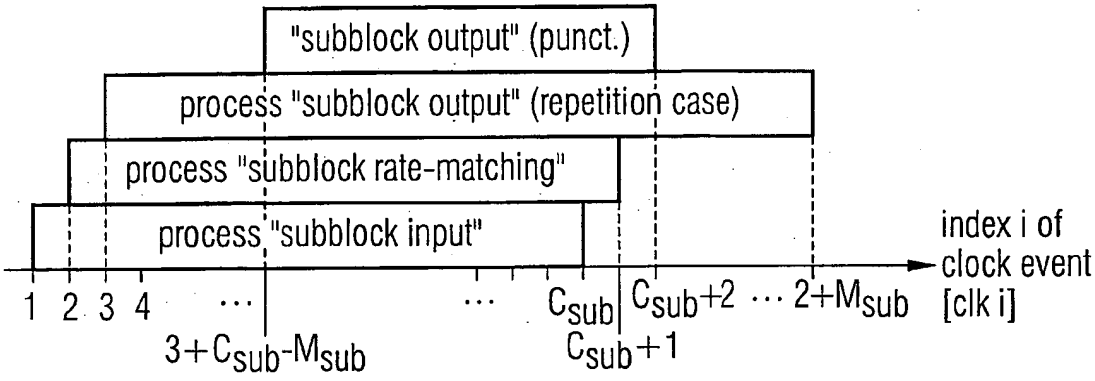

"subblock output" (punct.)
process "subblock output" (repetition case)
process "subblock rate-matching"
process "subblock input"
index i of clock event [clk i]
1 2 3 4 ... ... C_{sub} $C_{sub}+2$ ... $2+M_{sub}$
$3+C_{sub}-M_{sub}$
$C_{sub}+1$

FIG. 7

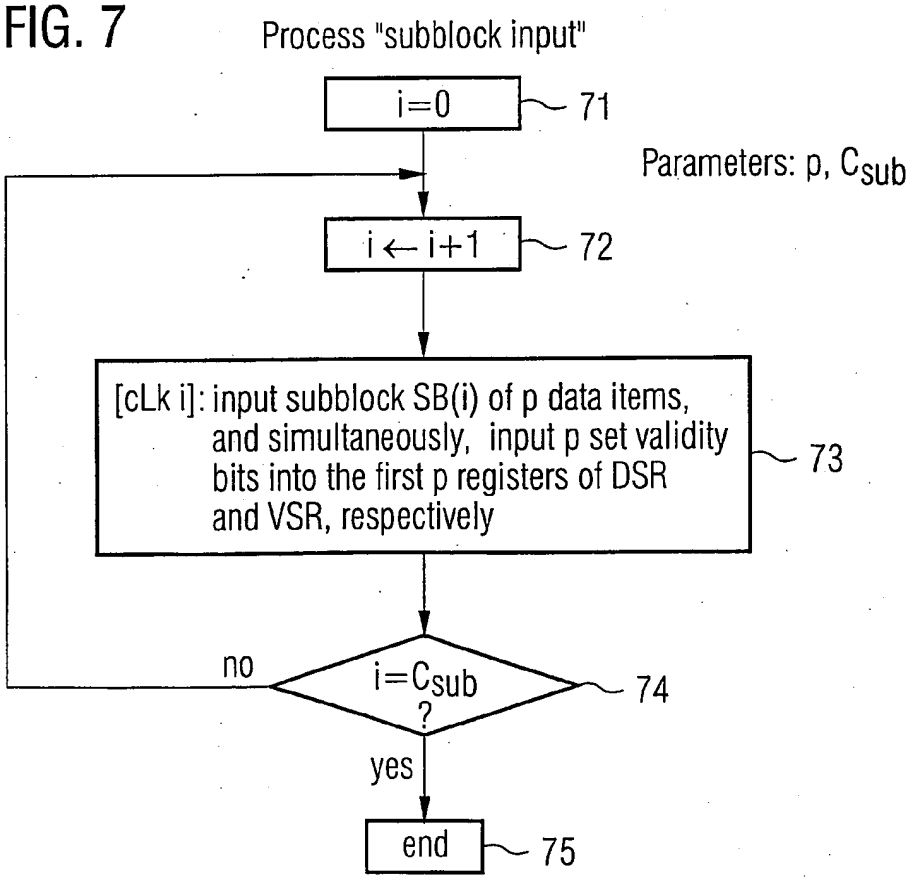

Process "subblock input"
i=0
71
Parameters: p, C_{sub}
i ← i+1
72
[cLk i]: input subblock SB(i) of p data items, and simultaneously, input p set validity bits into the first p registers of DSR and VSR, respectively
73
no
i=C_{sub} ?
74
yes
end
75

FIG. 8

Process "subblock rate matching"

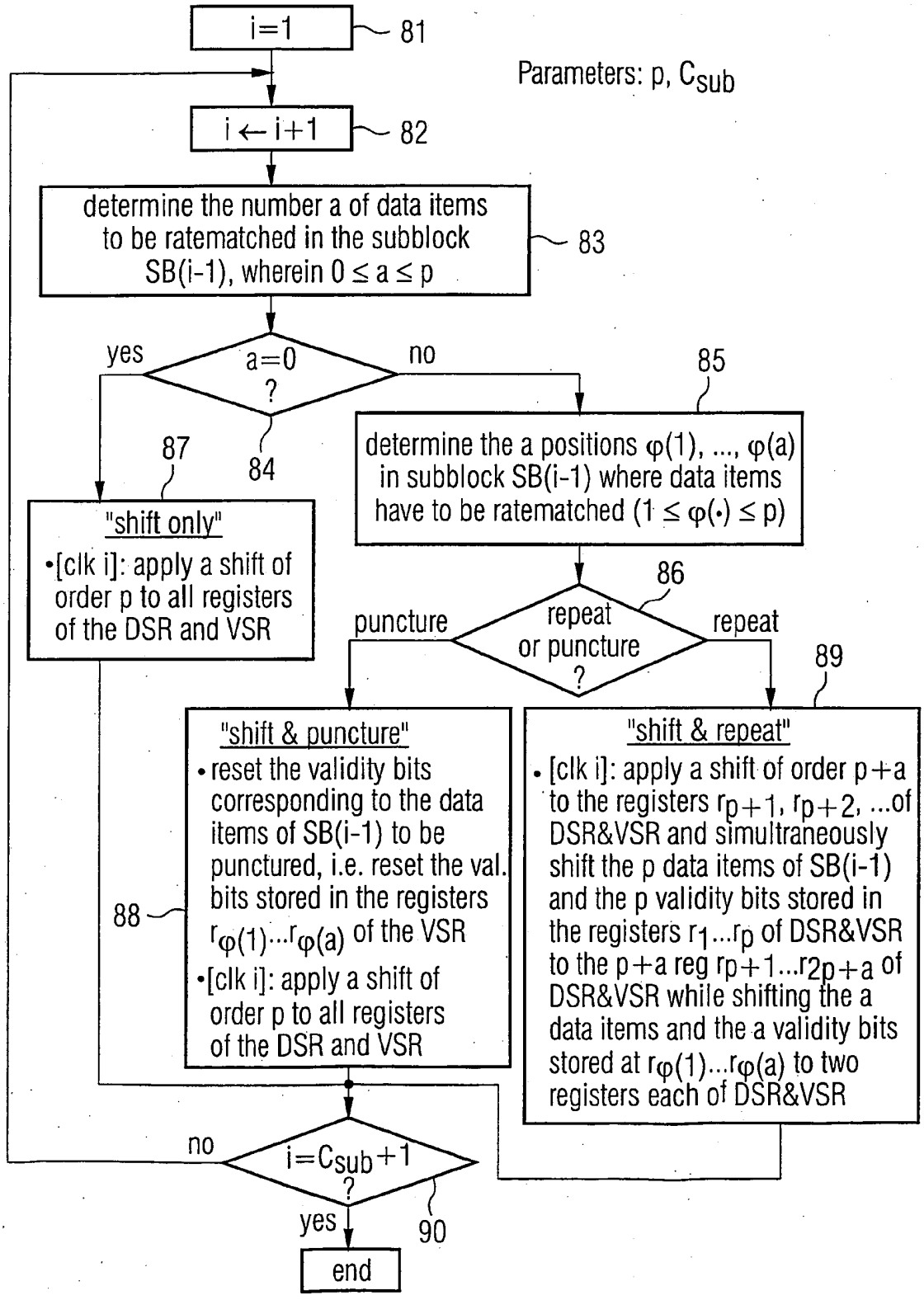
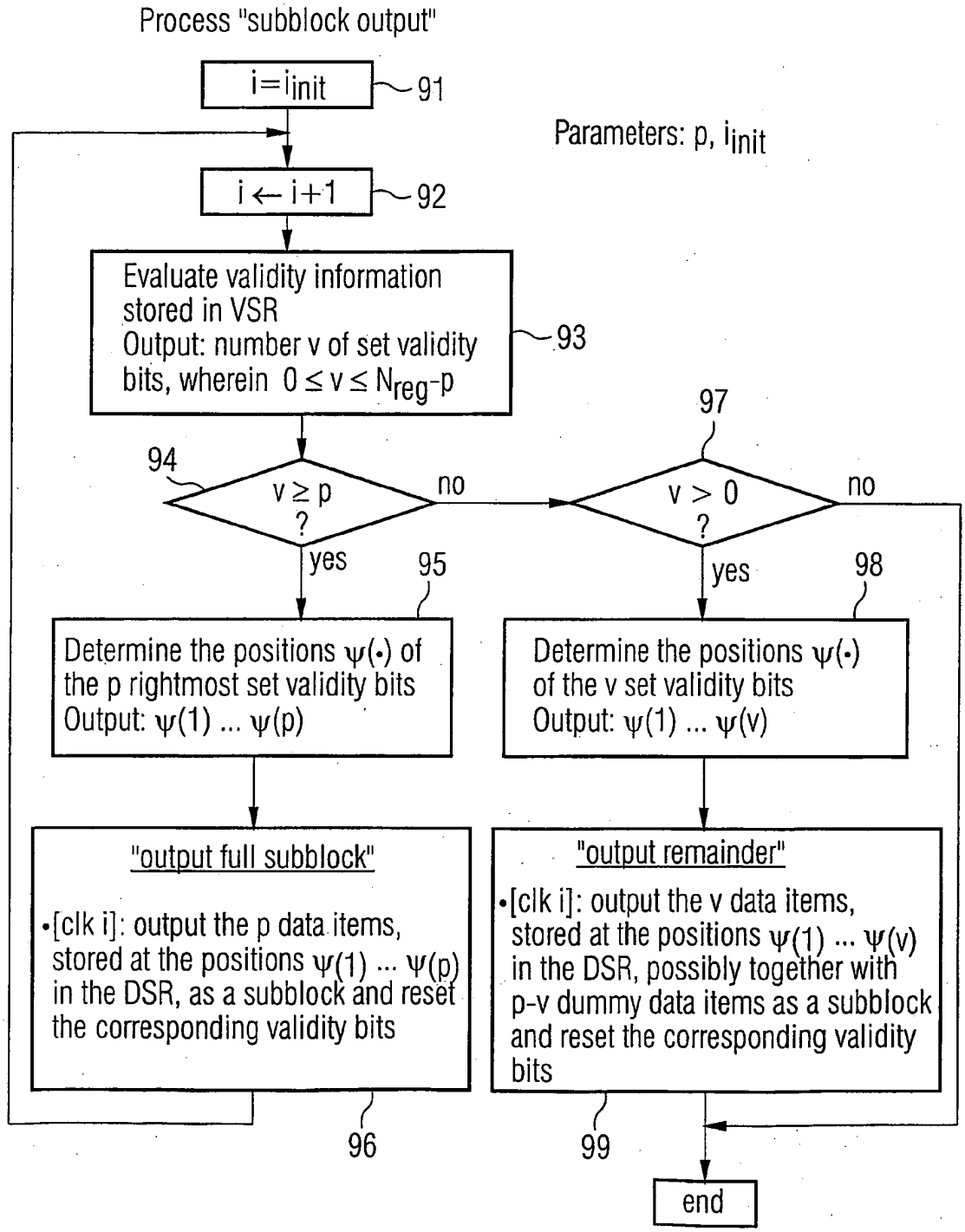


FIG. 9


Process "subblock output"
i=i_init
91
Parameters: p, i_init
i ← i+1
92
Evaluate validity information stored in VSR
Output: number v of set validity bits, wherein 0 ≤ v ≤ N_reg-p
93
97
94
v ≥ p ?
no
v > 0 ?
no
yes
95
yes
98
Determine the positions ψ(•) of the p rightmost set validity bits
Output: ψ(1) ... ψ(p)
Determine the positions ψ(•) of the v set validity bits
Output: ψ(1) ... ψ(v)
"output full subblock"
•[clk i]: output the p data items, stored at the positions ψ(1) ... ψ(p) in the DSR, as a subblock and reset the corresponding validity bits
"output remainder"
•[clk i]: output the v data items, stored at the positions ψ(1) ... ψ(v) in the DSR, possibly together with p-v dummy data items as a subblock and reset the corresponding validity bits
96
99
end

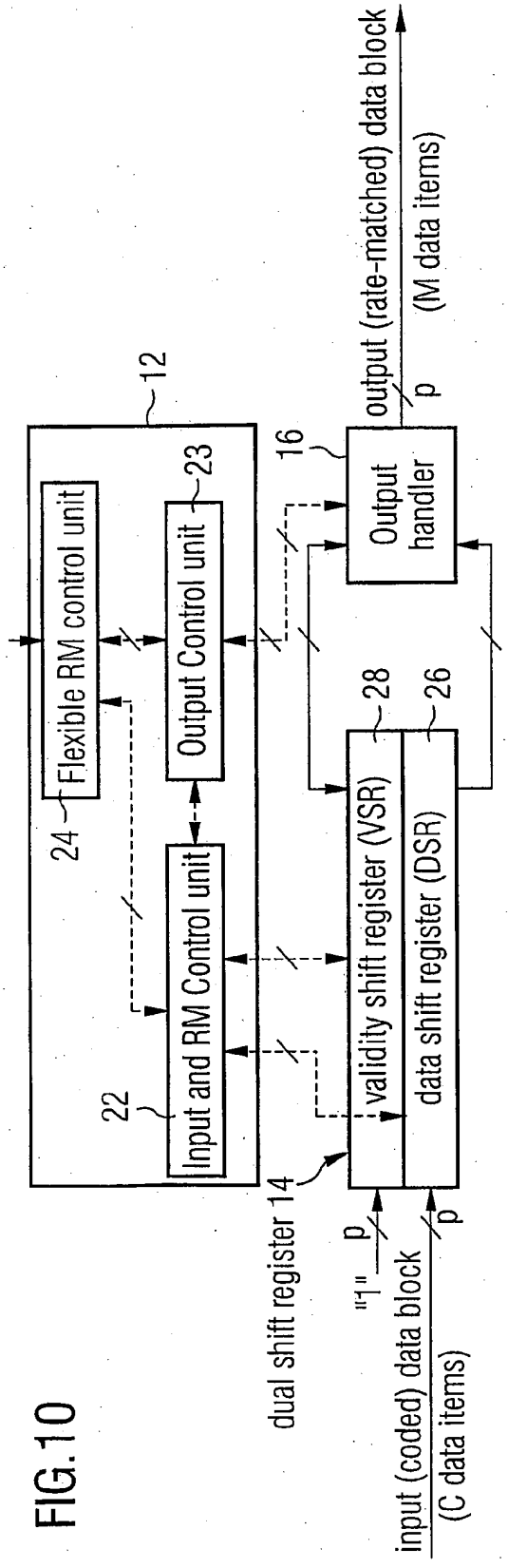

12
Flexible RM control unit
24
Output Control unit
23
Input and RM Control unit
22
16
Output handler
output (rate-matched) data block
p (M data items)
28
validity shift register (VSR)
26
data shift register (DSR)
dual shift register 14
"1" p
input (coded) data block
p
(C data items)

FIG.10

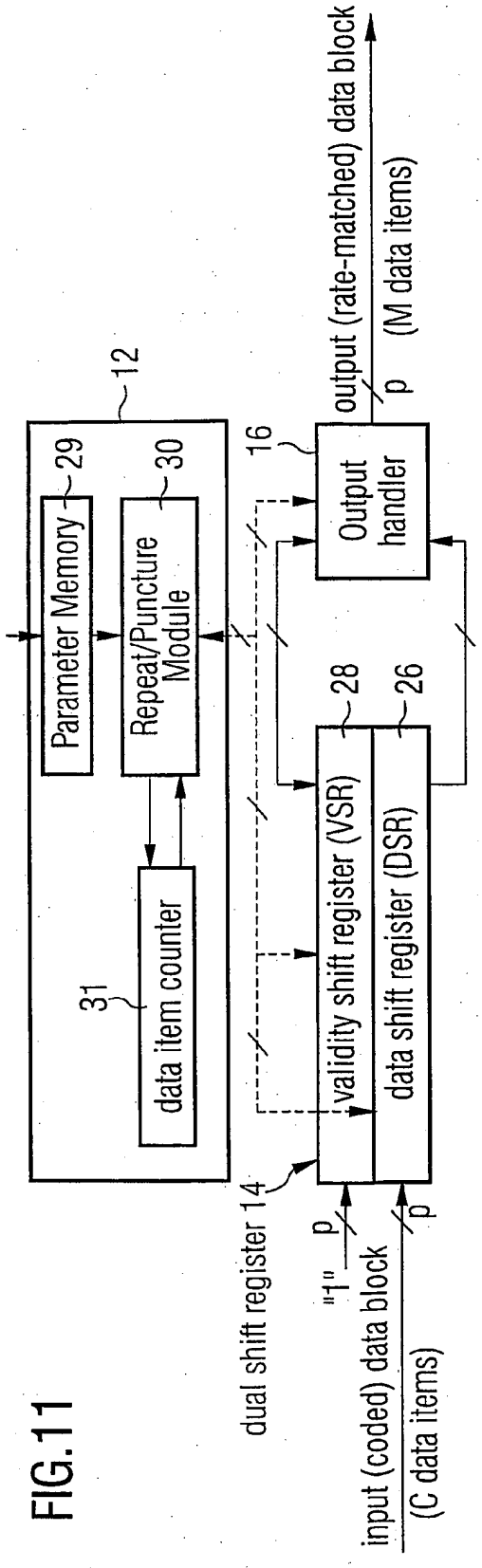

12
Parameter Memory
29
Repeat/Puncture Module
30
31
data item counter
16
Output handler
output (rate-matched) data block
p (M data items)
28
validity shift register (VSR)
26
data shift register (DSR)
dual shift register 14
"1" p
input (coded) data block
p
(C data items)

FIG.11

FIG.12a

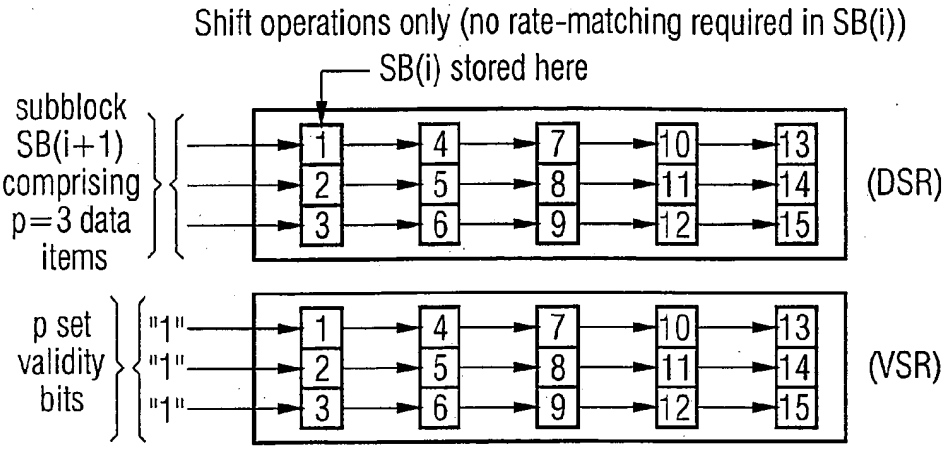


FIG.12b

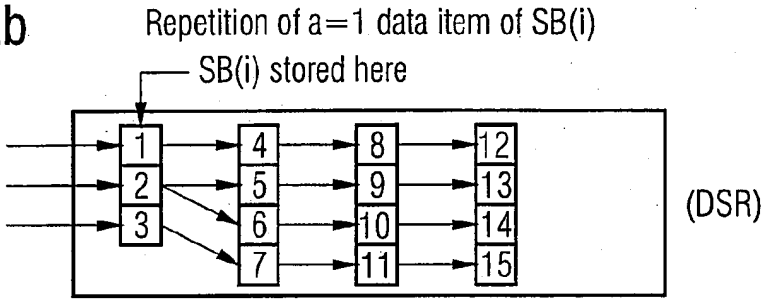
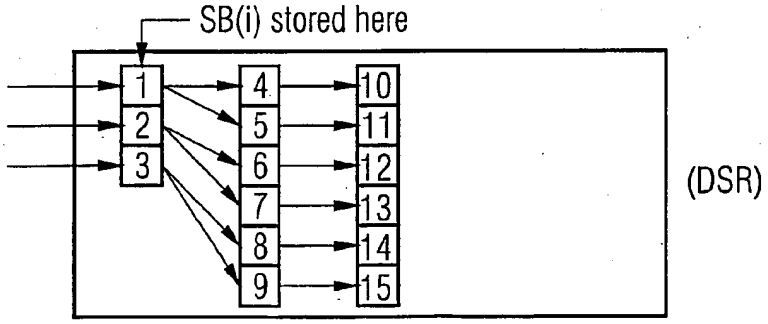


FIG.12c



Legend:

- □ : register (memory location) of DSR and VSR, respectively
- j : j-th register of DSR/VSR (r_j)
- j → k : shift from register j to register k at [clk i+1]
- j → k, l : shift from register j to register k and l (repetition) at [clk i+1]

FIG.13

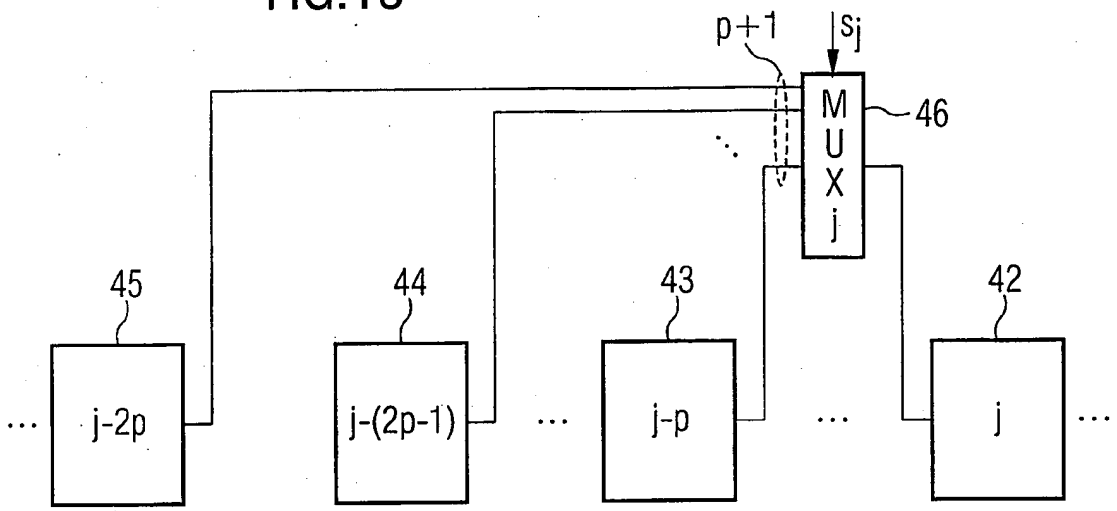
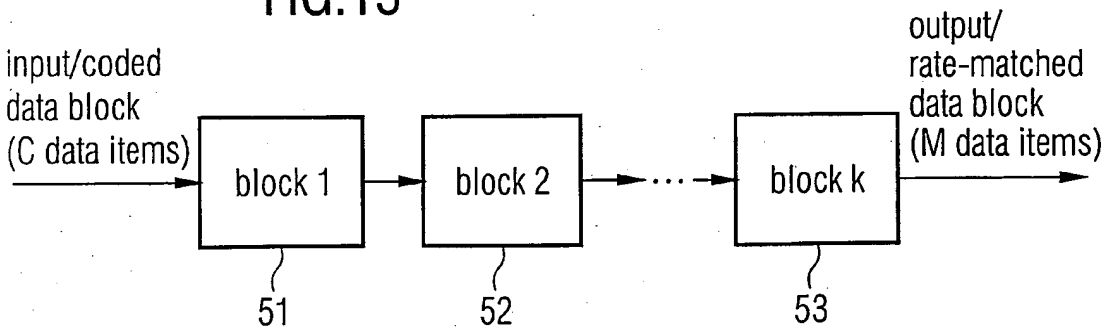

p+1
sj
MUX j
46
45
44
43
42
j-2p
j-(2p-1)
j-p
j

FIG.15


input/coded data block (C data items)
block 1
block 2
block k
output/ rate-matched data block (M data items)
51
52
53

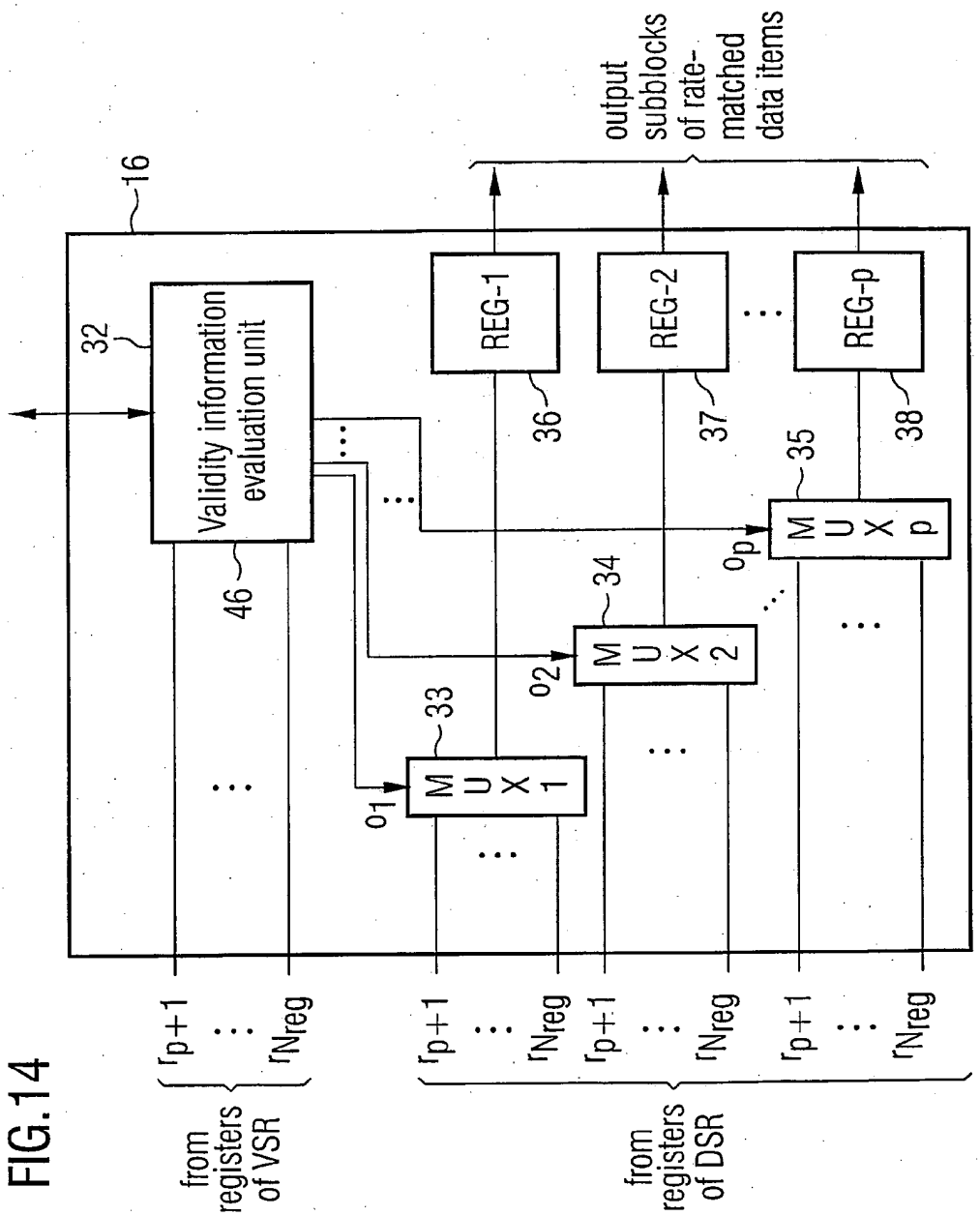

output subblocks of rate-matched data items
16
32
Validity information evaluation unit
46
REG-1
REG-2
REG-p
36
37
38
35
34
33
MUX 1
MUX 2
MUX p
o1
o2
op
from registers of VSR
from registers of DSR
rp+1
rNreg

FIG.14

FIG.16a

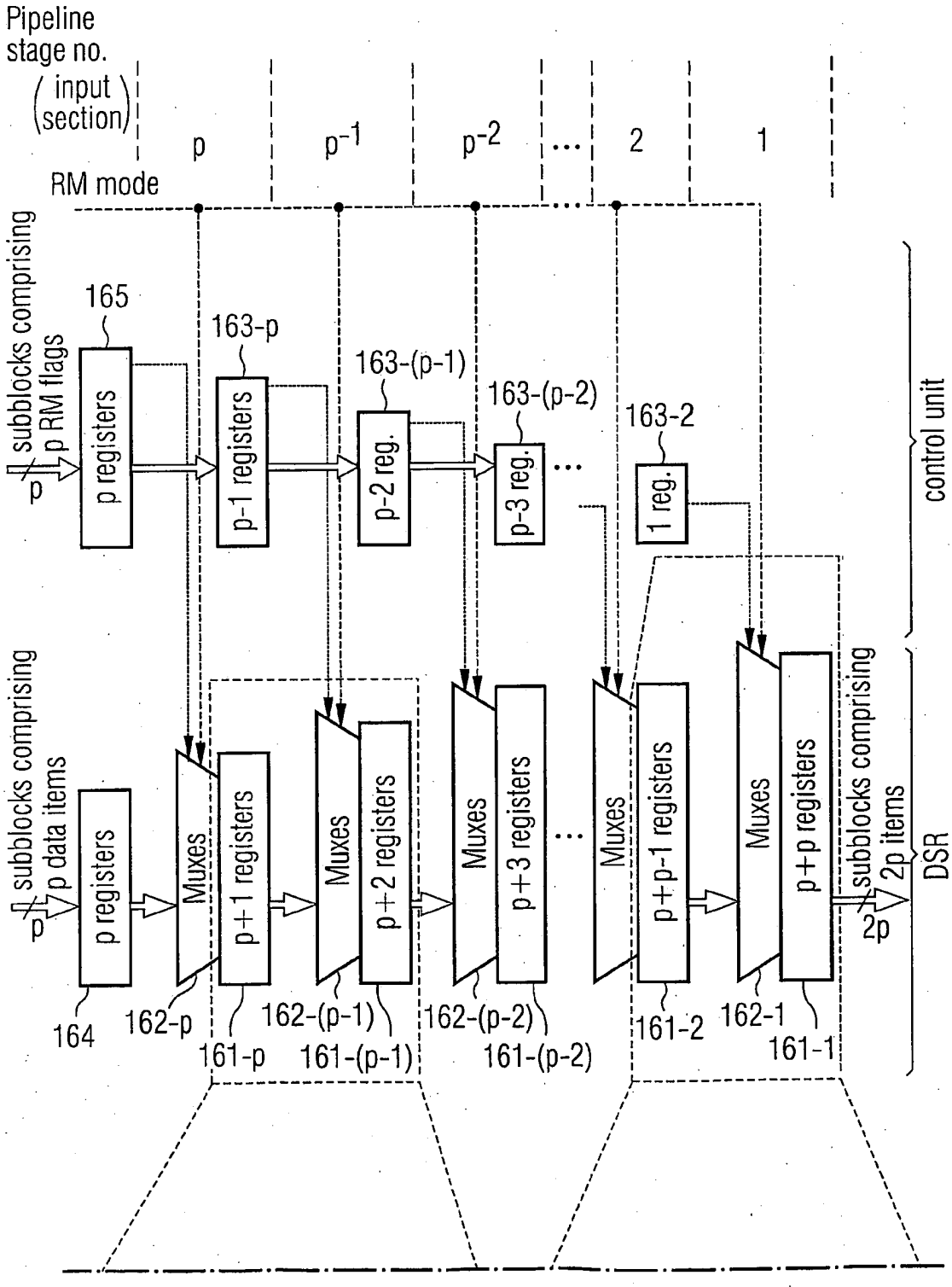
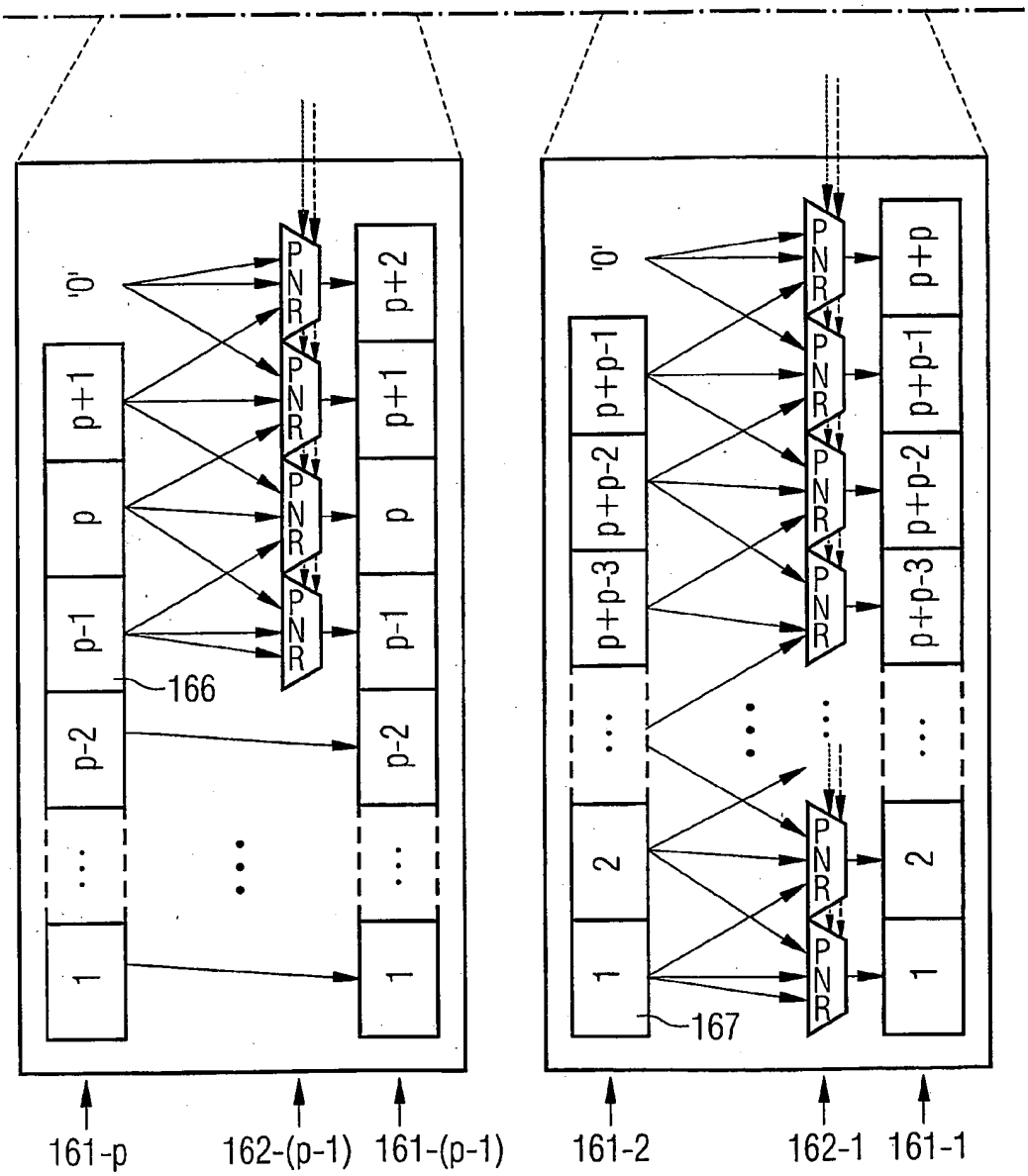

Pipeline stage no.
input section
p
p-1
p-2
...
2
1
RM mode
subblocks comprising p RM flags
p
165
p registers
163-p
p-1 registers
163-(p-1)
p-2 reg.
163-(p-2)
p-3 reg.
163-2
1 reg.
control unit
subblocks comprising p data items
p
p registers
Muxes
p+1 registers
Muxes
p+2 registers
Muxes
p+3 registers
Muxes
p+p-1 registers
Muxes
p+p registers
subblocks comprising 2p items
2p
DSR
164
162-p
161-p
162-(p-1)
161-(p-1)
162-(p-2)
161-(p-2)
161-2
162-1
161-1

FIG.16b

FIG.16c



Legend:

- [j] : j-th register of DSR
- ▷ : multiplexer

FIG.17a

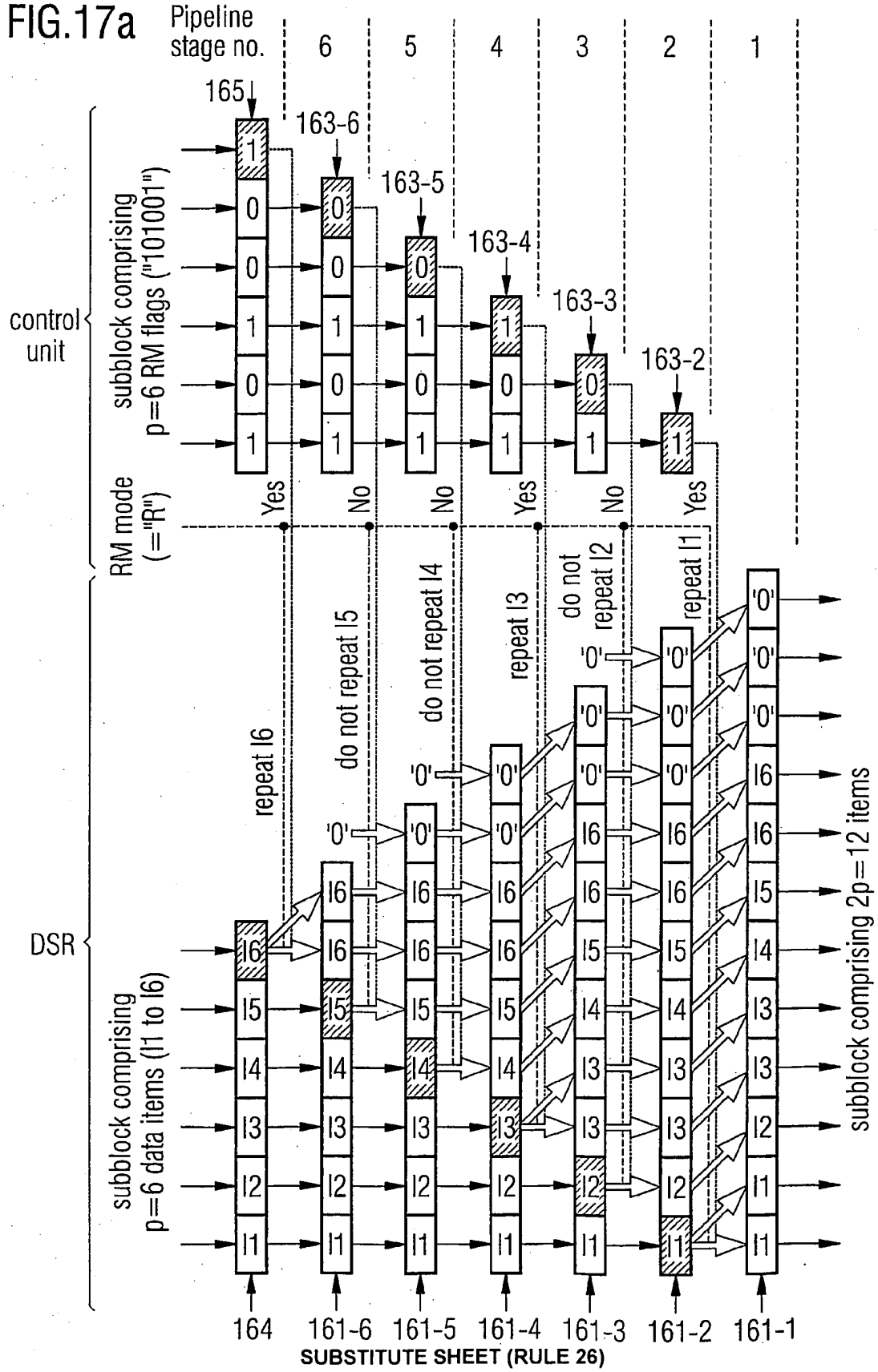

Pipeline stage no.
6
5
4
3
2
1
165
163-6
163-5
163-4
163-3
163-2
control unit
subblock comprising p=6 RM flags ("101001")
RM mode (="R")
Yes
No
No
Yes
No
Yes
DSR
subblock comprising p=6 data items (I1 to I6)
repeat I6
do not repeat I5
do not repeat I4
repeat I3
do not repeat I2
repeat I1
subblock comprising 2p=12 items
164
161-6
161-5
161-4
161-3
161-2
161-1

FIG.17b

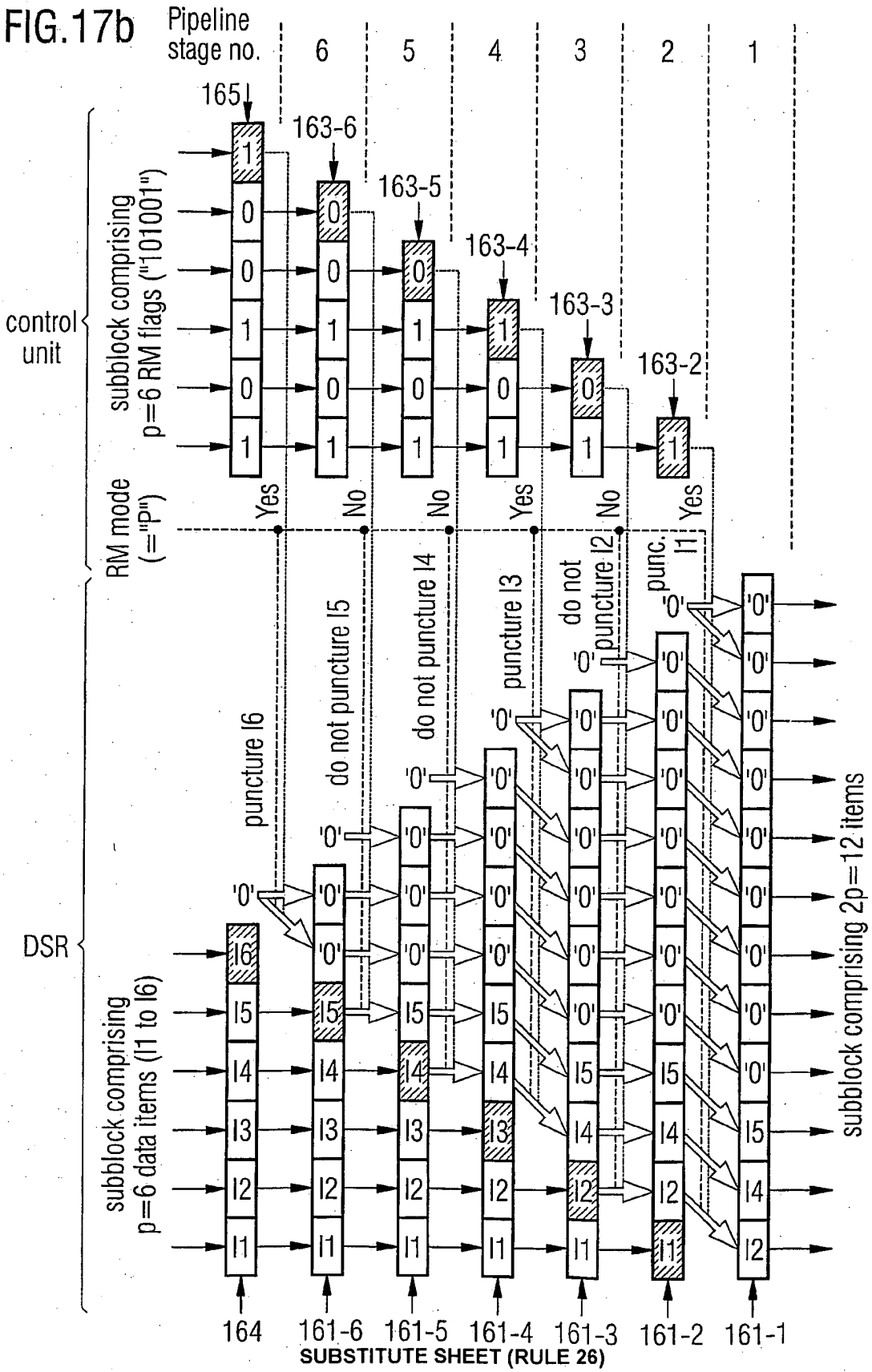
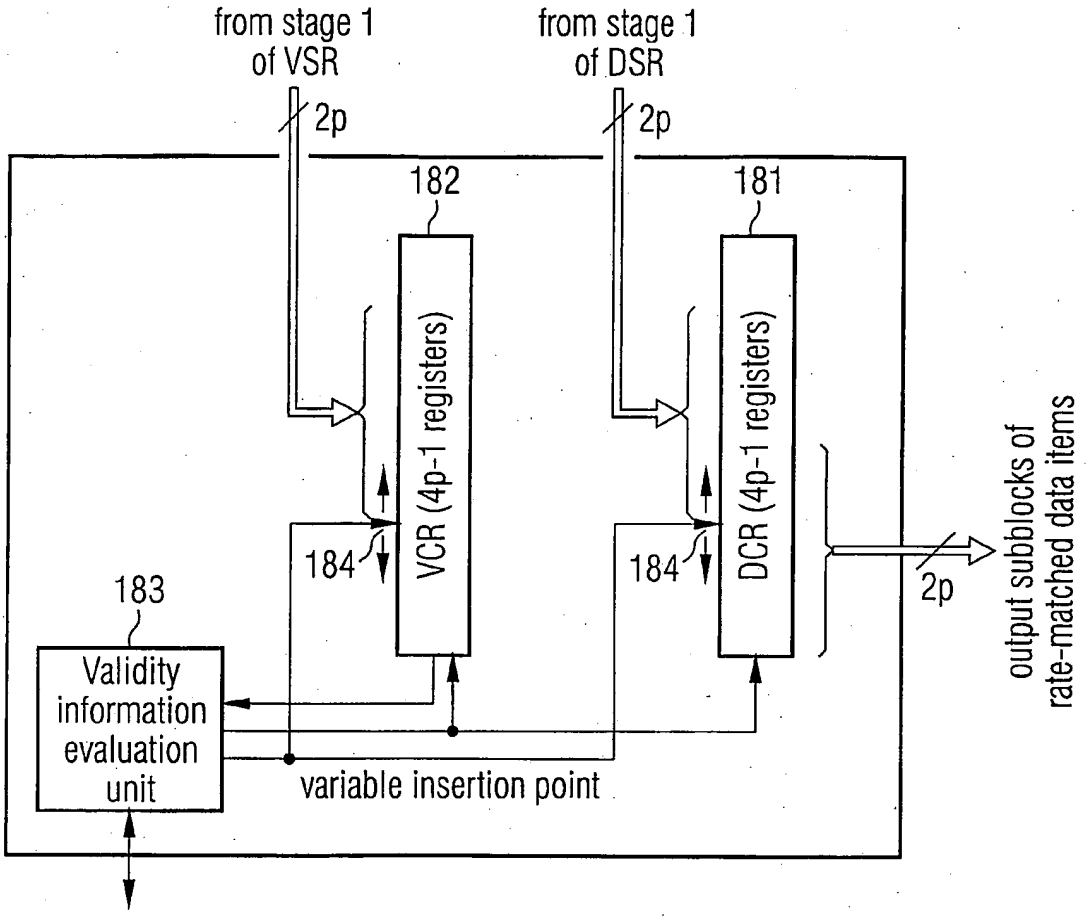

Pipeline stage no.
6
5
4
3
2
1
165
163-6
163-5
163-4
163-3
163-2
control unit
subblock comprising p=6 RM flags ("101001")
RM mode (="P")
Yes
No
No
Yes
No
Yes
DSR
subblock comprising p=6 data items (I1 to I6)
puncture I6
do not puncture I5
do not puncture I4
puncture I3
do not puncture I2
punc. I1
subblock comprising 2p=12 items
164
161-6
161-5
161-4
161-3
161-2
161-1

FIG.18a


from stage 1 of VSR
from stage 1 of DSR
2p
2p
182
181
VCR (4p-1 registers)
DCR (4p-1 registers)
184
184
183
Validity information evaluation unit
variable insertion point
2p
output subblocks of rate-matched data items

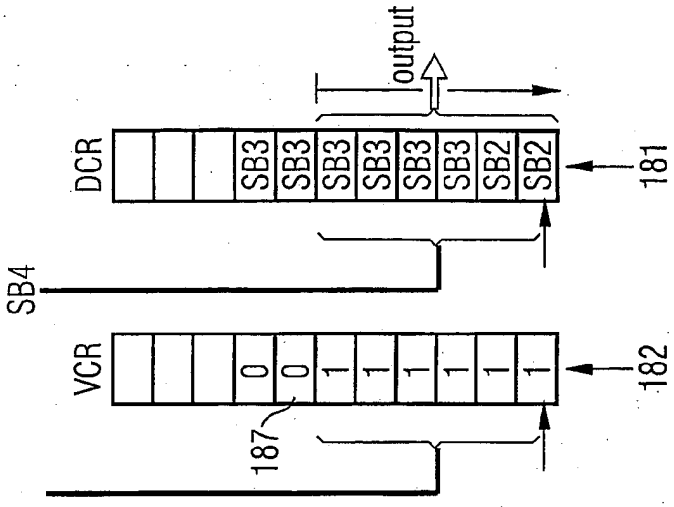


FIG.18d

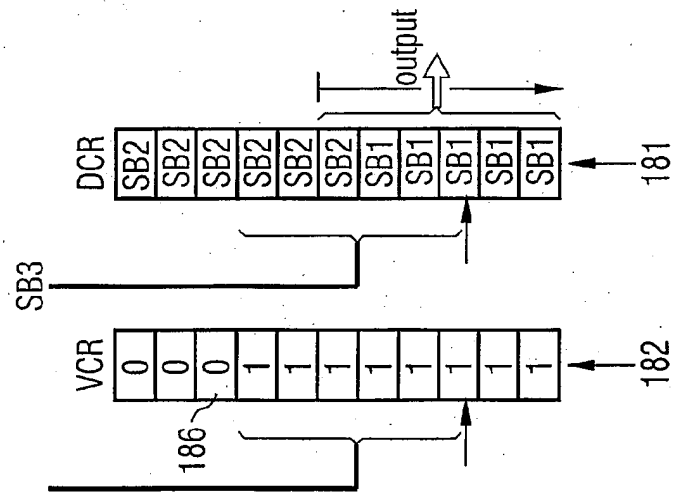


FIG.18c

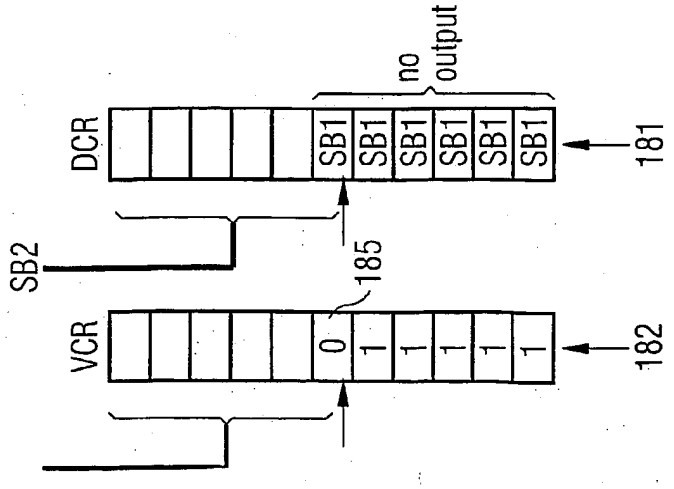


FIG.18b